**Mux, Adder & Subtractor Using ModelSim**

**LAB # 10**

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**Fall 2021**

**CSE304L Computer Organization & Architecture**

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Class Section: **B**

Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Prof: Ammad khalil**

February 14, 2022

**Department of Computer Systems Engineering**

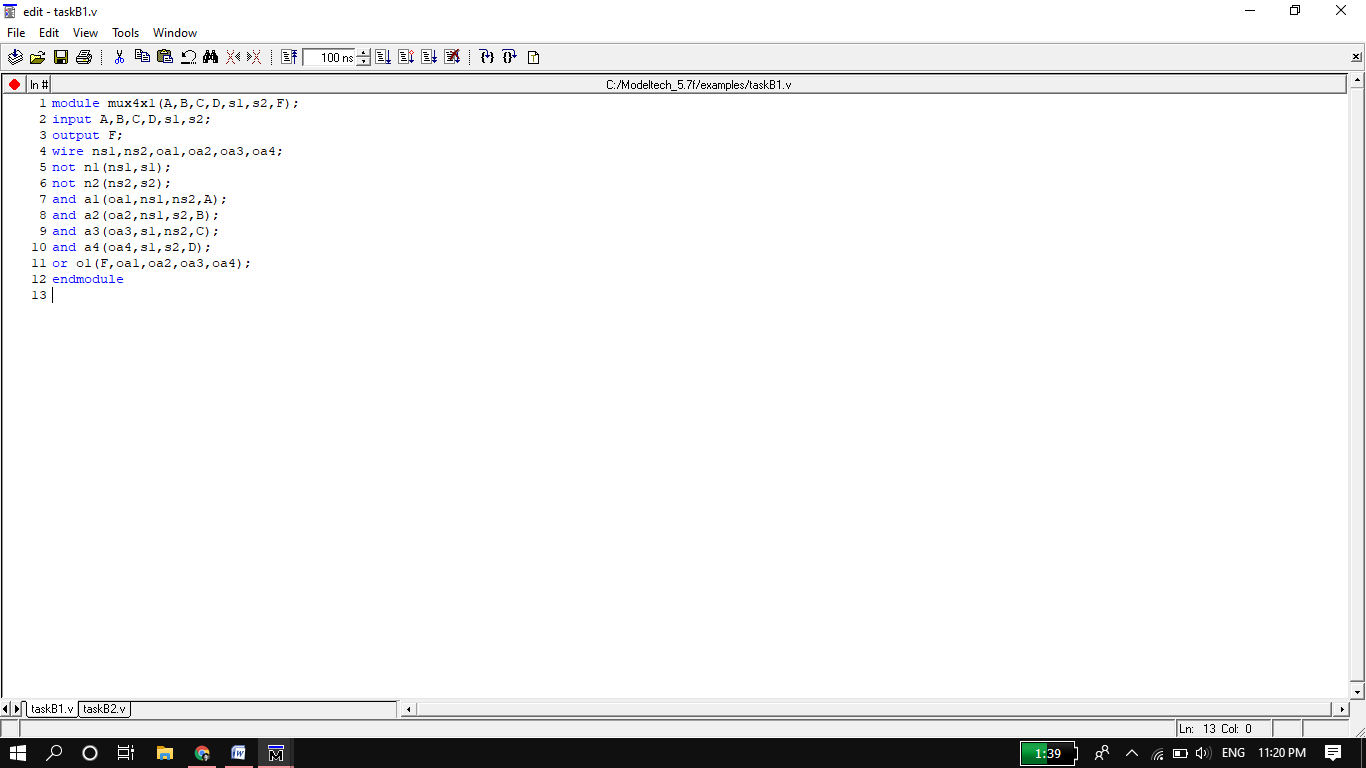
**University of Engineering and Technology, Peshawar**

**Objective:**

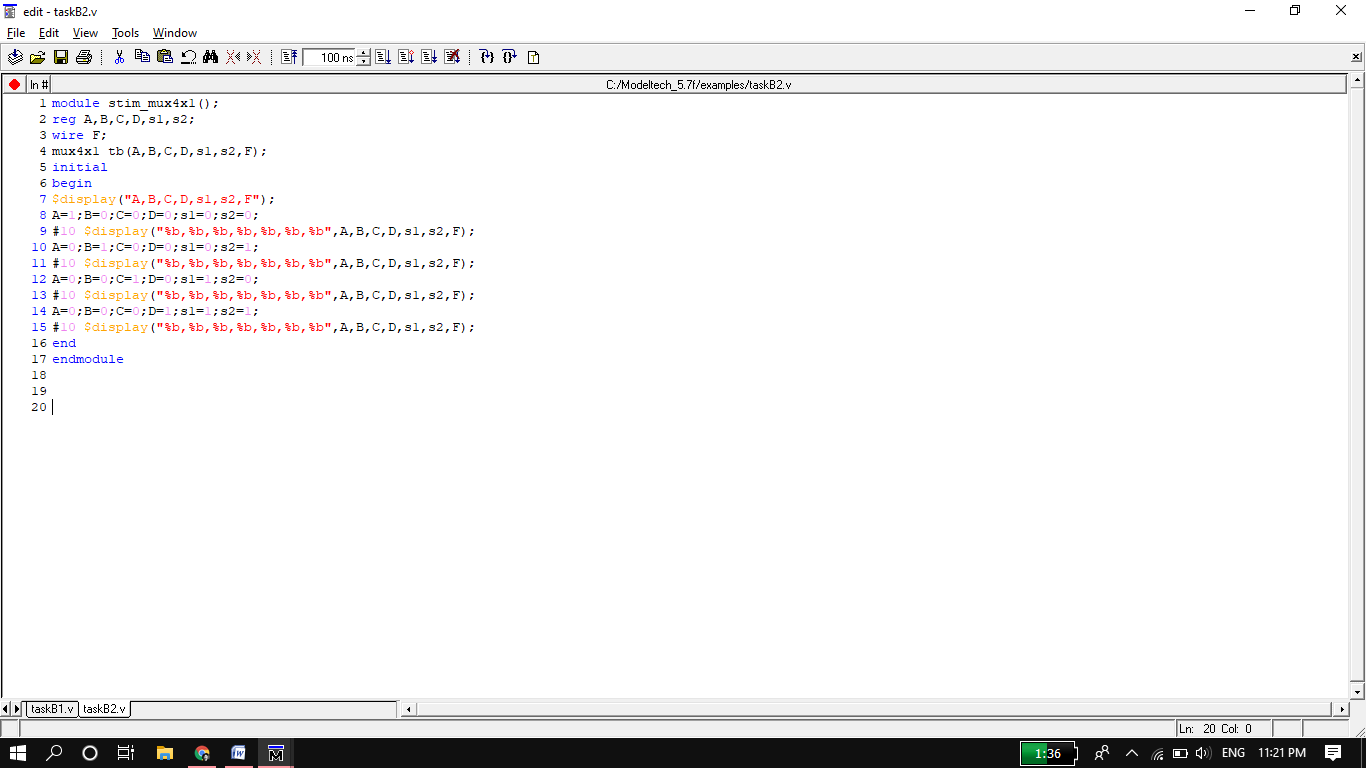
* To know how to implement Mux, Adder and subtractor using verilog HDL.

**Task01: implement 4x1 Multiplexer.**

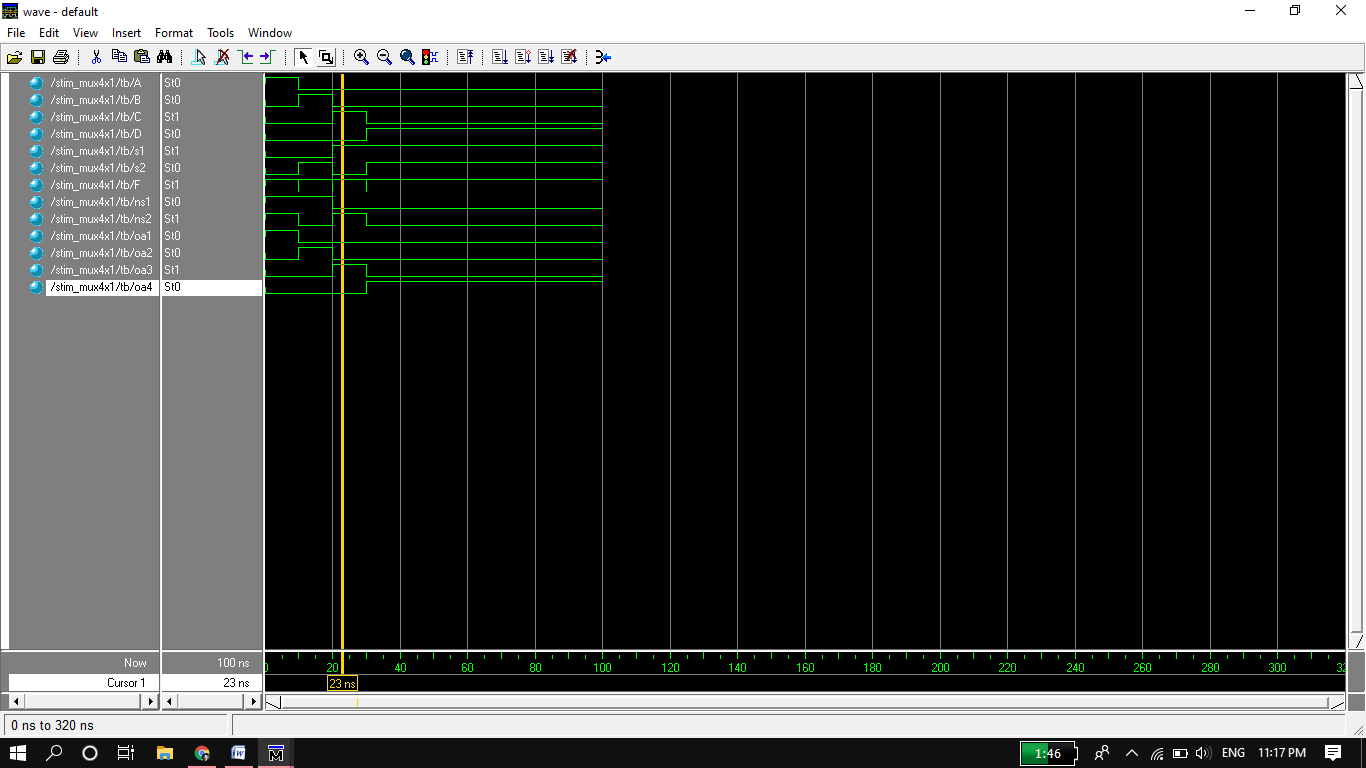
**Logic Code:**



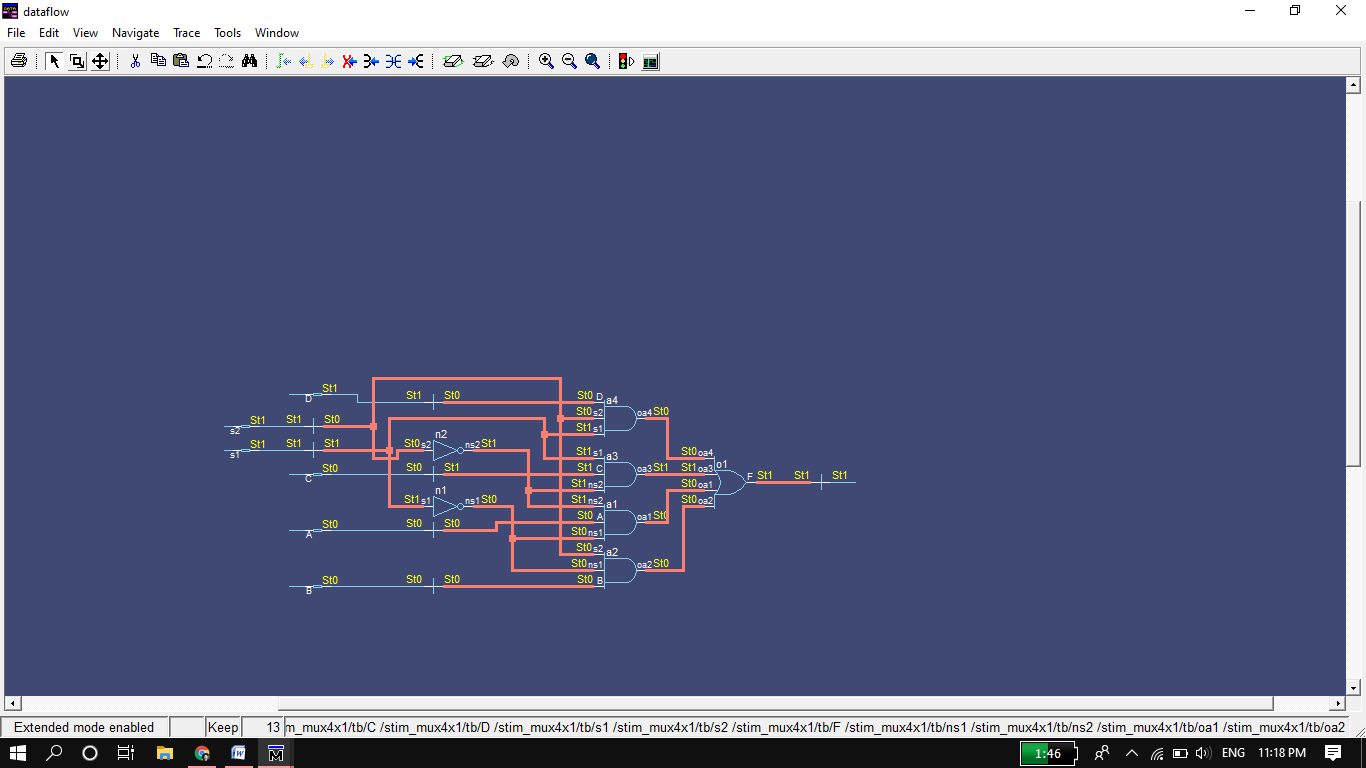
**Test bench file:**



**Wave Form output:**

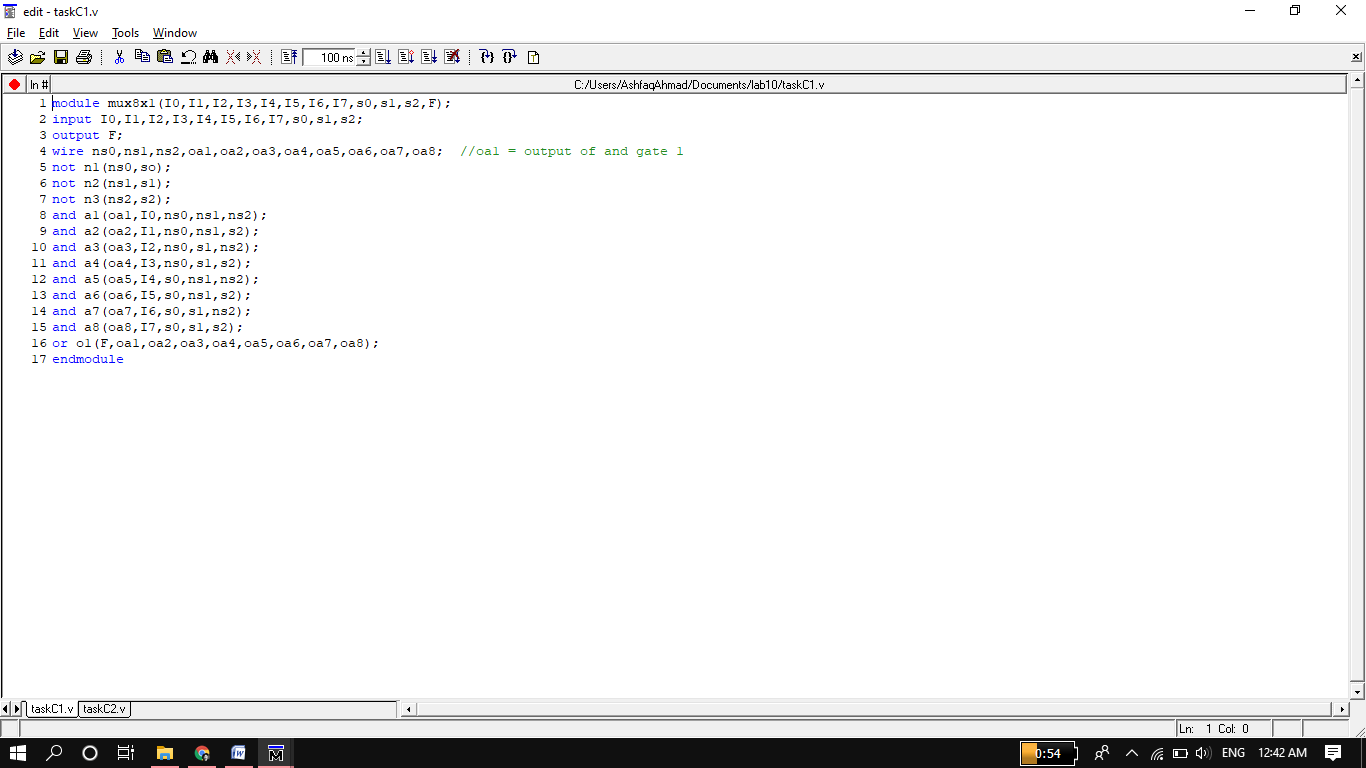


**Circuit:**

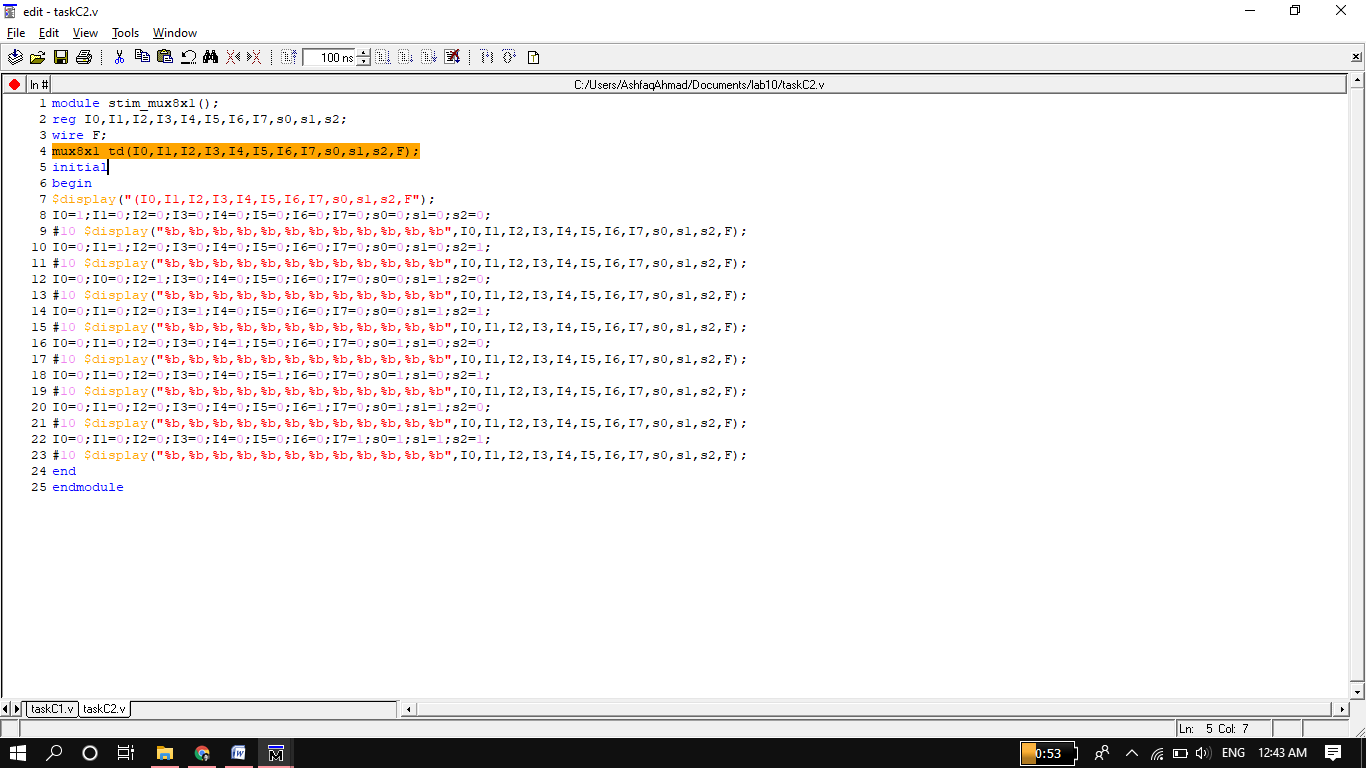


**Task02: implement 8x1 Multiplexer.**

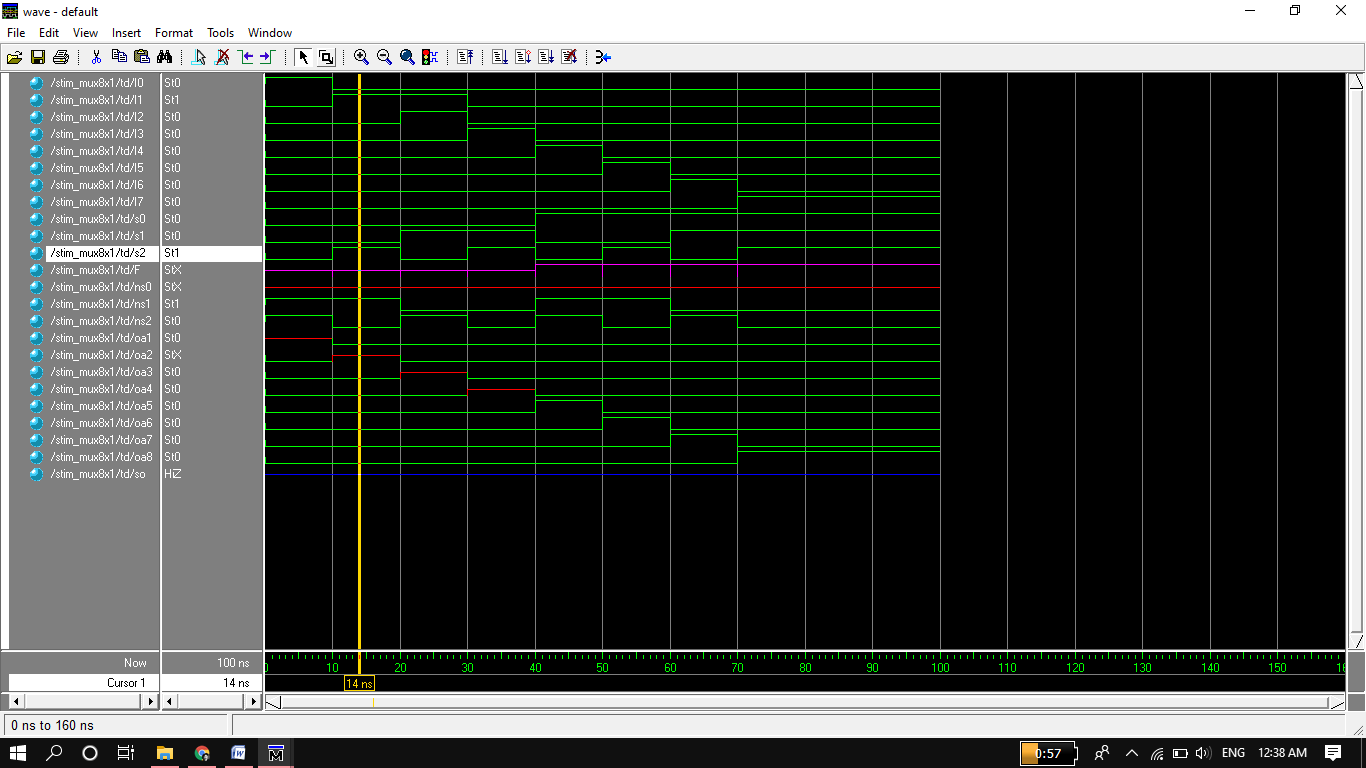
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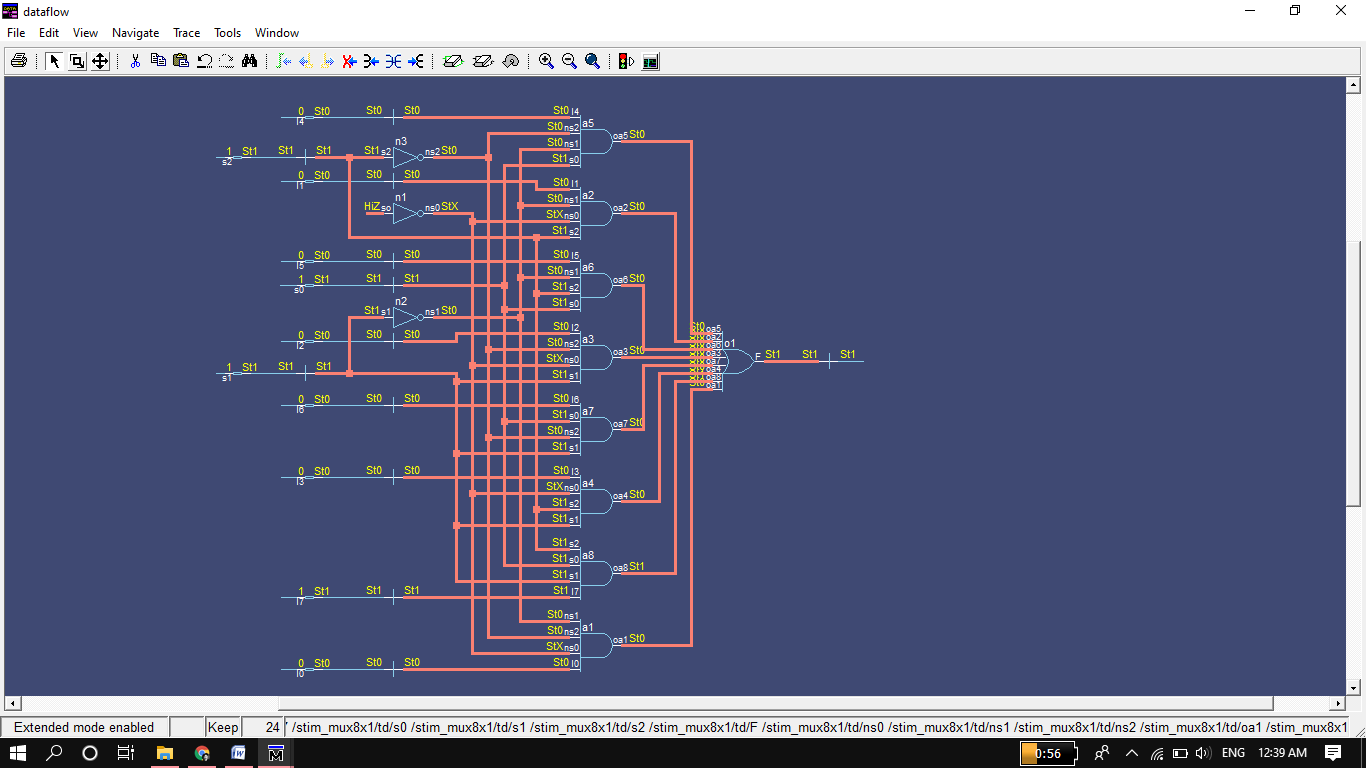
**Test bench file:**



**Wave Form output:**

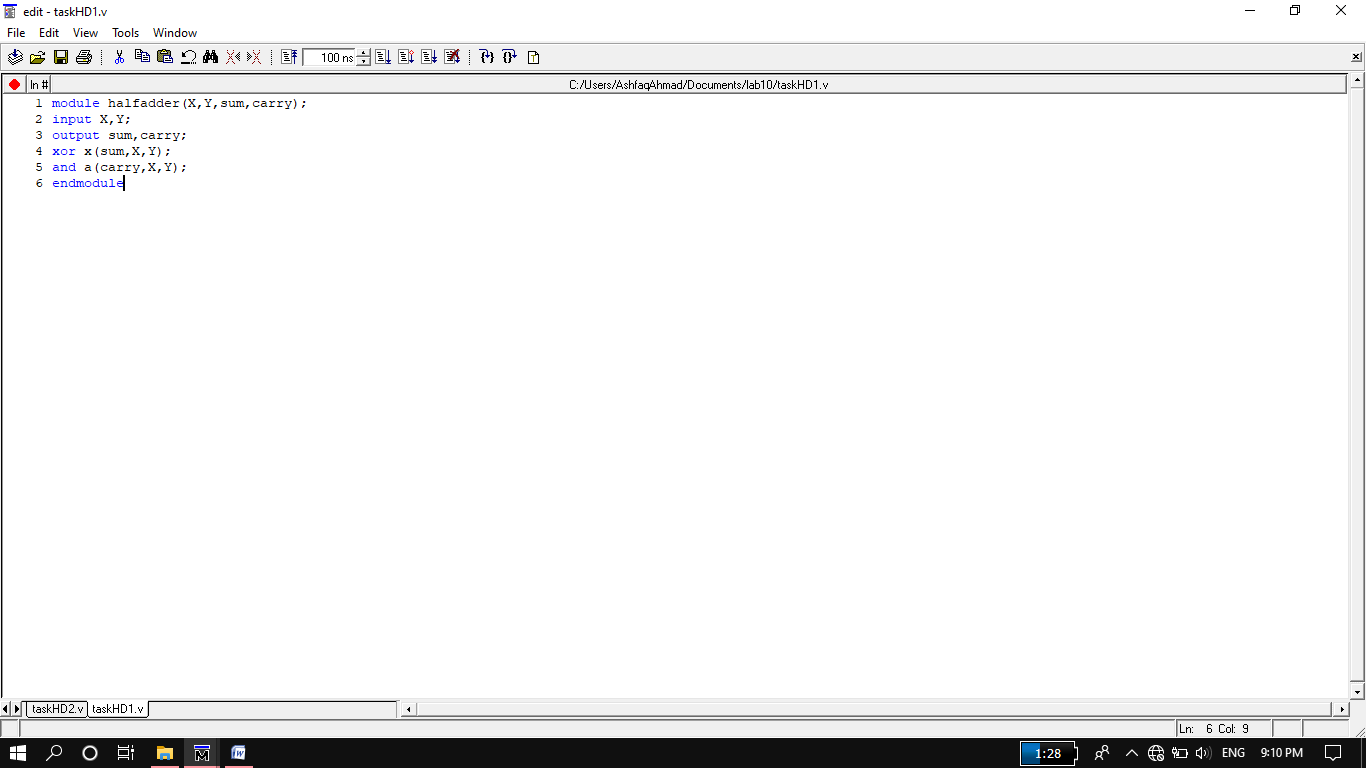


**Circuit:**

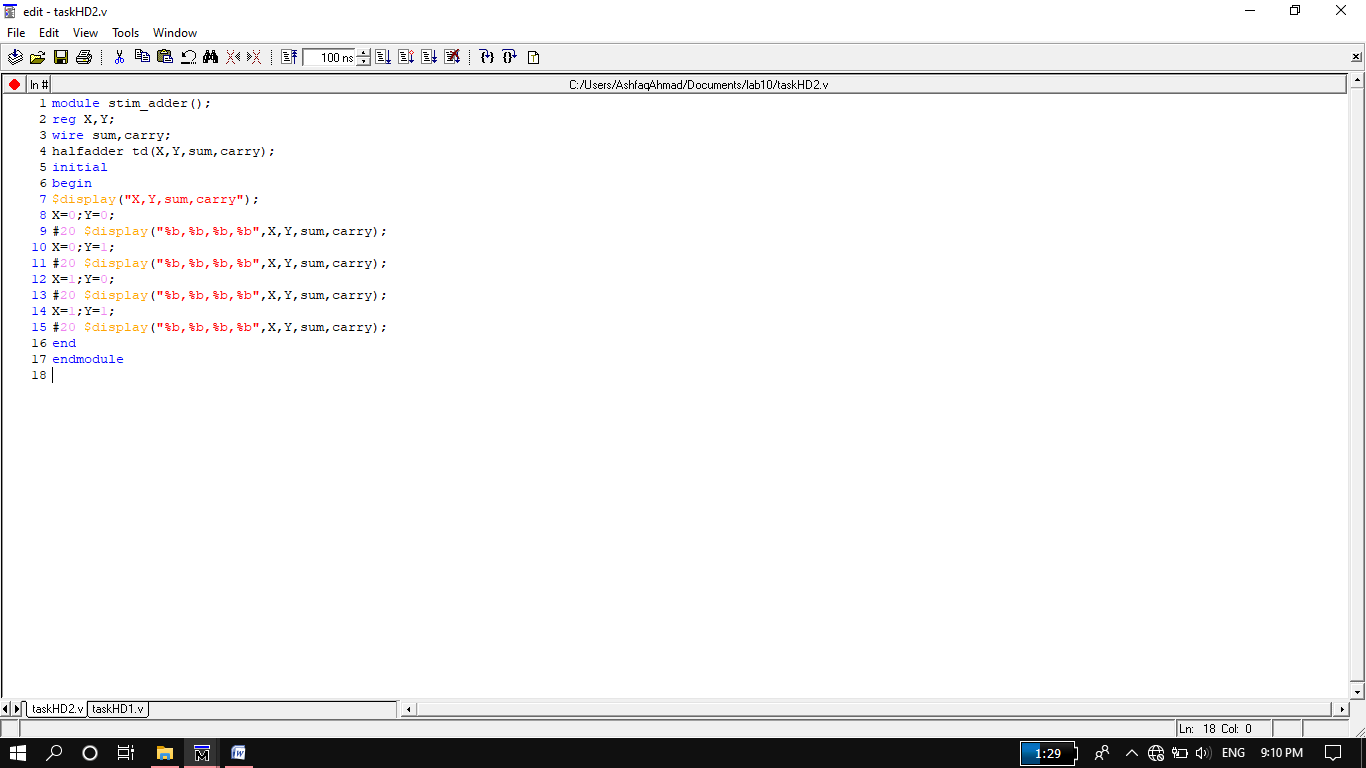


**Task03: Half Adder.**

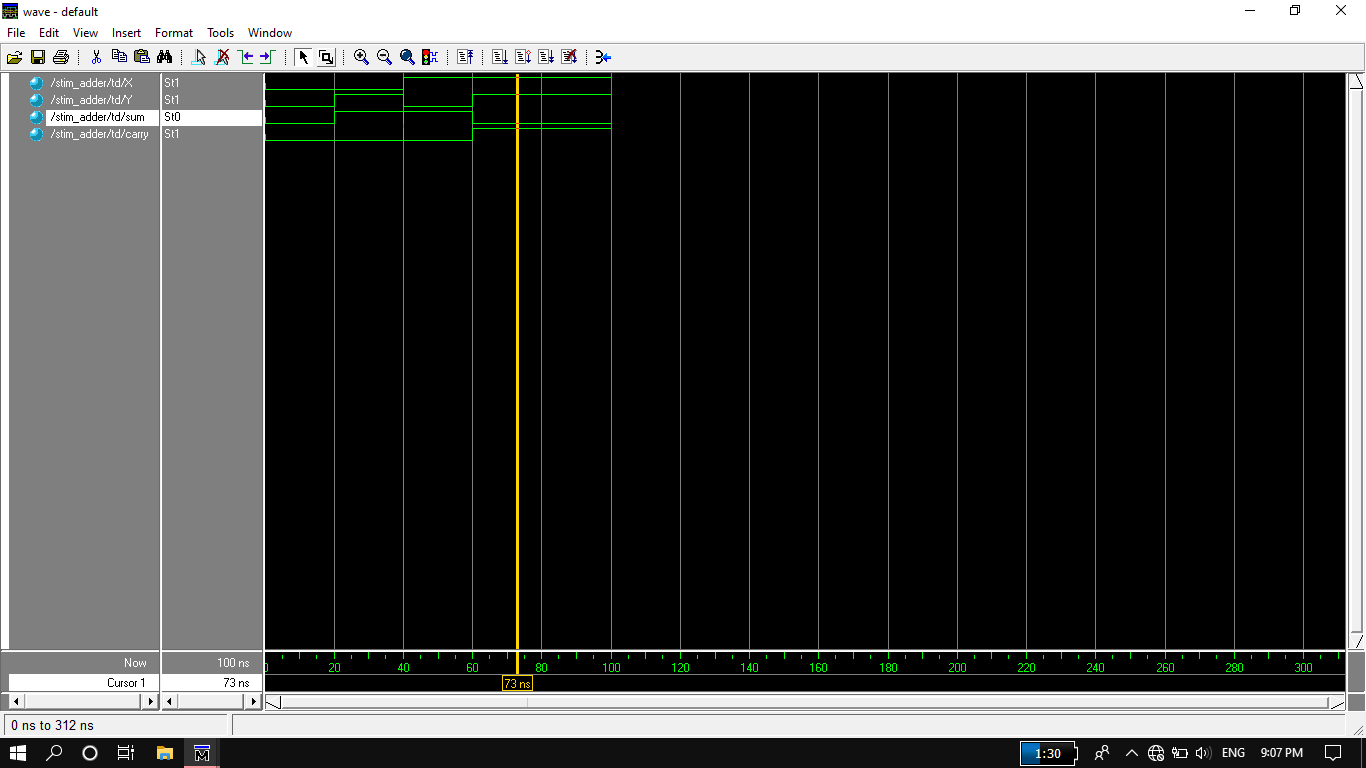
**Logic Code:**



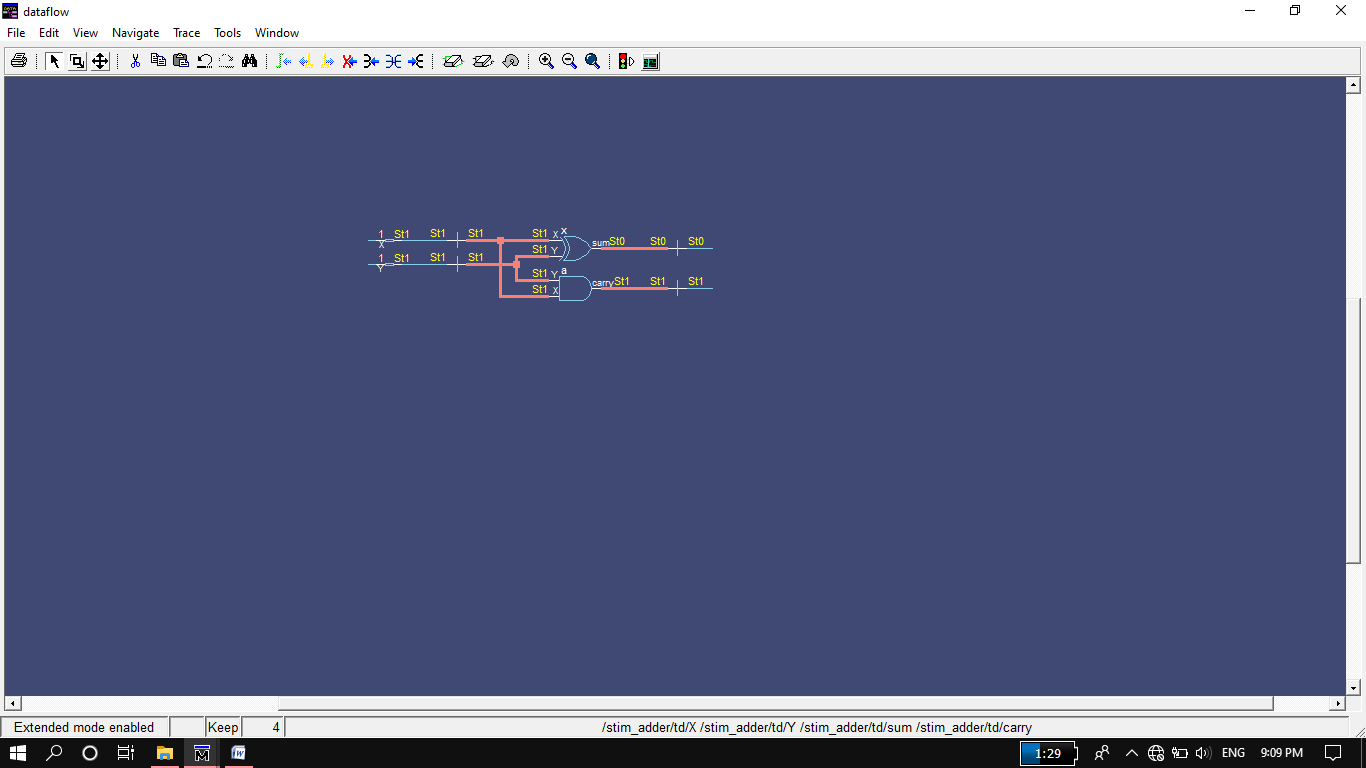
**Test bench file:**



**Wave Form output:**

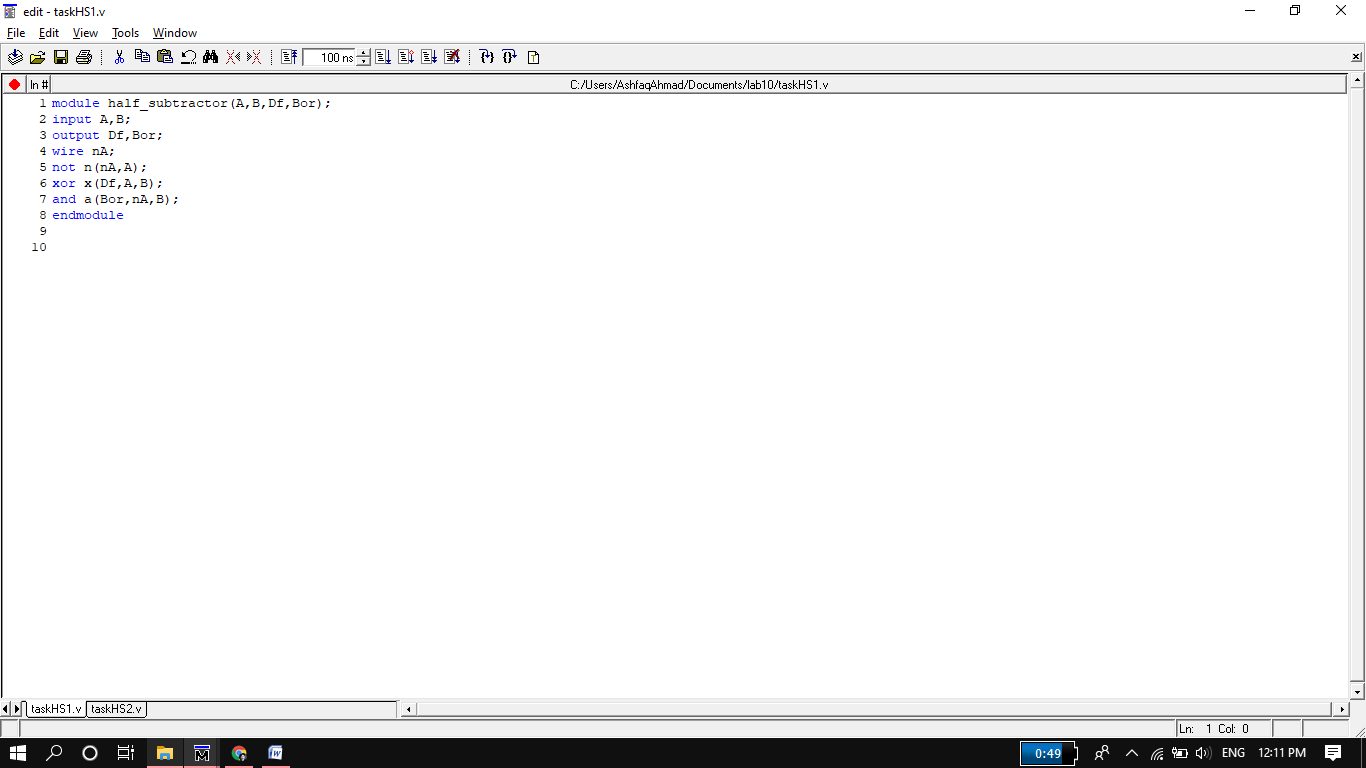


**Circuit:**

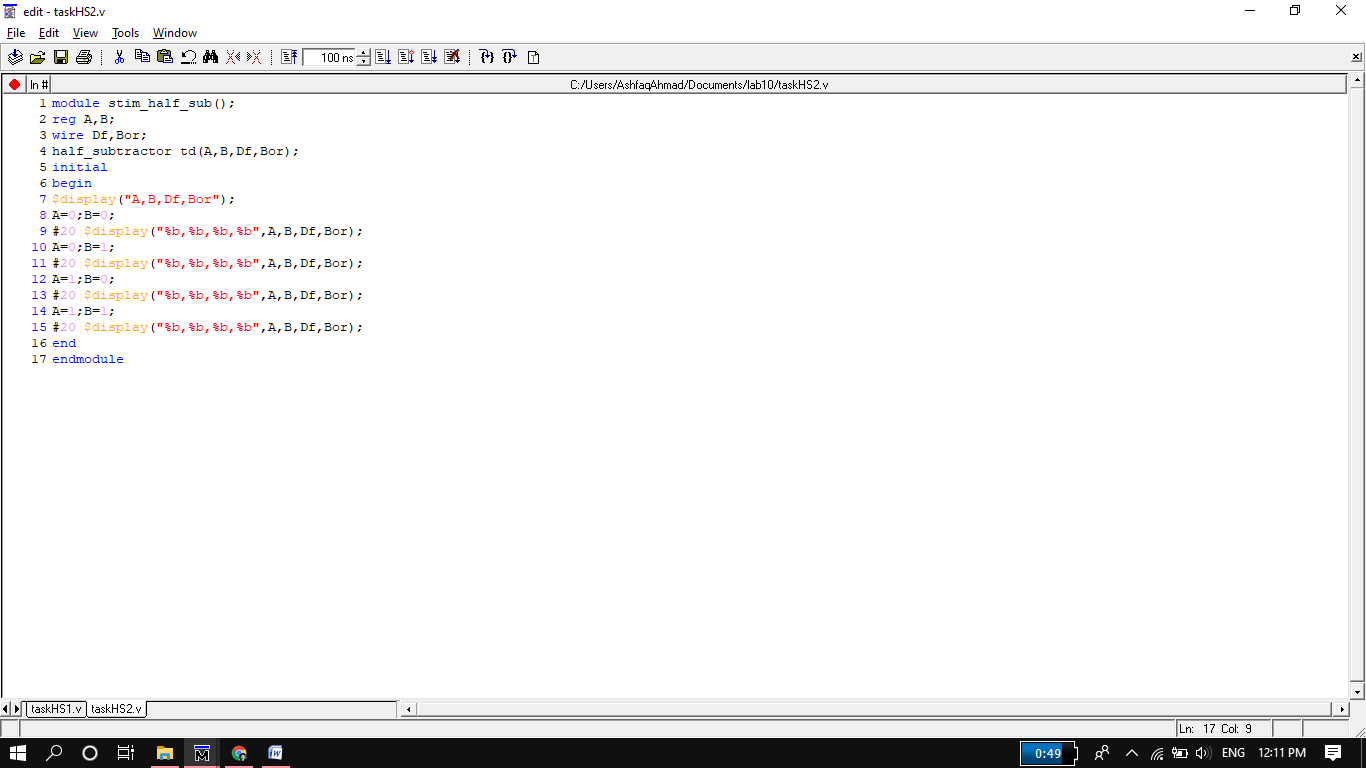


**Task04: implement Half Subtractor.**

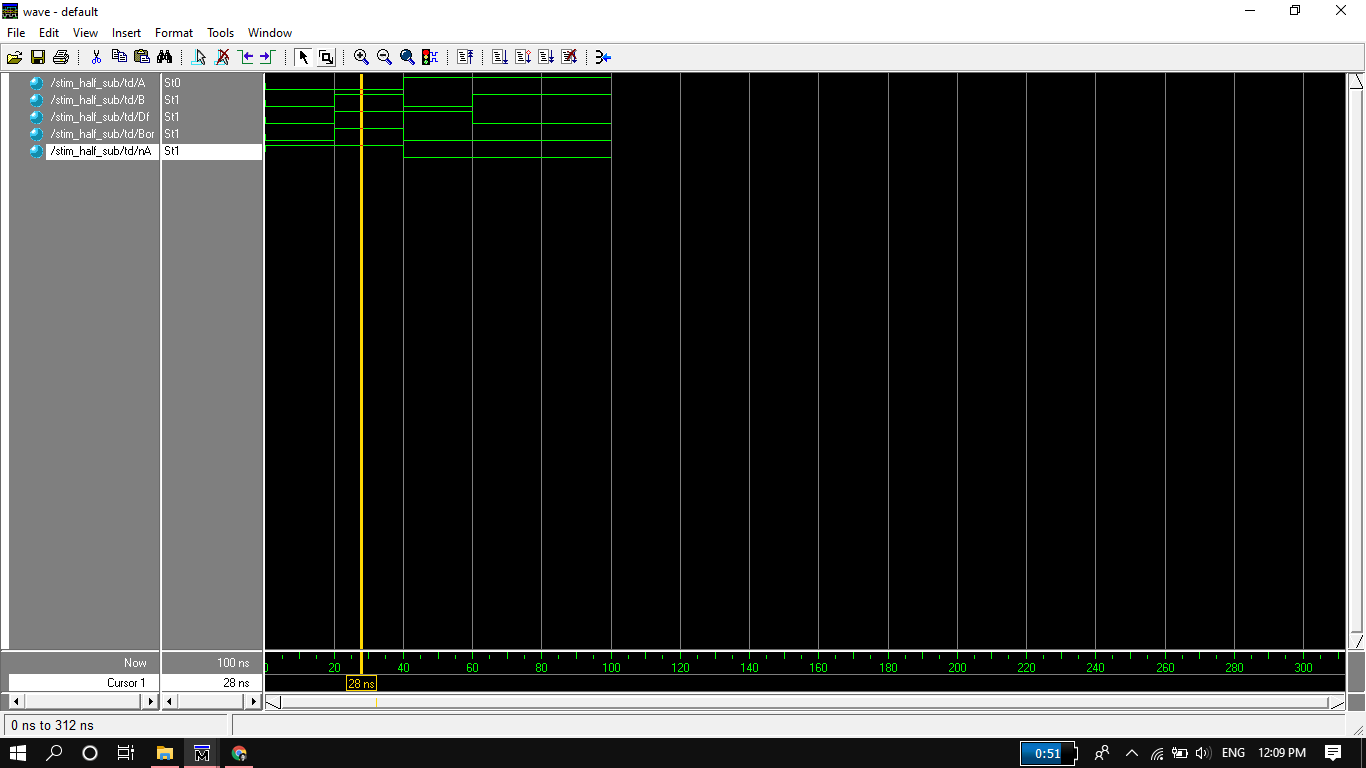
**Logic Code:**



**Test bench file:**



**Wave Form output:**



**Circuit:**

